AMENDED CLAIMS

1. (previously presented) A method of improving the efficiency of synchronizing a clock signal for an integrated circuit, comprising:

providing a clock input signal (CIN), an inverted clock input signal (CIN'), and a clock delay signal (CDLY);

detecting a plurality of phases of CIN and CDLY based on timing conditions associated with CIN and CDLY; and

selectively inputting CIN or CIN' into a synchronous mirror delay (SMD) based on the phase of CIN and CDLY to reduce a number of delay stages in the SMD.

2. (currently amended) The method of claim 1 wherein the timing conditions include a period of CIN (t_{ck}) and a period from a rising edge in CIN to a rising edge in CDLY (t_{mdl}), and ~~wherein~~ selectively inputting includes inputting CIN into the SMD when $t_{mdl} > t_{ck}/2$ and inputting CIN' into the SMD when $t_{mdl} < t_{ck}/2$ to reduce the number of delay stages in the SMD.

3. (original) The method of claim 2 wherein the number of delay stages in the SMD is reduced substantially in half.

4. (currently amended) The method of claim 2 wherein the SMD has a plurality of delay lines, and ~~wherein~~ the number of delay stages in at least one of the SMD delay lines is reduced substantially to 59 from 128.

5. (previously presented) A method of improving the efficiency of synchronizing a clock signal for an integrated circuit, comprising:

providing a clock input signal (CIN), an inverted clock input signal (CIN'), and a clock delay signal (CDLY), each signal having timing characteristics;

interposing a phase detector and selection system between an external clock signal and a synchronous mirror delay (SMD);

determining which of a number of phases the signals are based on the timing characteristics; and

selectively directing the signals based upon the phase of the signals.

6. (previously presented) The method of claim 5 wherein selectively directing includes selectively directing CIN or CIN' to the SMD based upon the timing characteristics of CIN and CDLY.

7. (previously presented) The method of claim 5 wherein selectively directing includes bypassing CIN or CIN' from the SMD based upon the timing characteristics of CIN and CDLY.

8. (previously presented) The method of claim 5 further including defining the timing characteristics as a period of CIN as t_{ck} and defining a period from a rising edge in CIN to a rising edge in CDLY as t_{mdl}, and wherein determining includes determining that the phases include:

a first phase when $t_{mdl} > t_{ck}/2$;

a second phase when $t_{mdl} < t_{ck}/2$;

a third phase when $t_{mdl} = t_{ck}$; and

a fourth phase when $t_{mdl} = t_{ck}/2$.

9. (previously presented) A method of synchronizing a clock signal for an integrated circuit, comprising:

providing an internal clock signal (CIN), an inverted internal clock signal (CIN'), and a clock delay signal (CDLY) having timing characteristics;

differentiating, with a phase detector, a plurality of phases based upon the timing characteristics of CIN and CDLY; and

selecting, based on the phases, one of CIN and CIN' to be input into a synchronous mirror delay (SMD) thereby reducing a number of delay stages in the SMD.

10. (currently amended) A method of synchronizing a clock signal for an integrated circuit, comprising:

providing an internal clock signal (CIN), an inverted internal clock signal (CIN'), and a clock delay signal (CDLY) having timing characteristics;

determining a plurality of phases based upon the timing characteristics of CIN and CDLY; and

for at least one phase, directing CIN' into a synchronous mirror delay (SMD) such that a reduced number of delay stages are achieved.

11. (currently amended) The method of claim 10 wherein the timing characteristics define a period of CIN as t_{ck} and also define from a rising edge in CIN to a rising edge in CDLY as t_{mdl}, and ~~wherein~~ directing occurs when $t_{mdl} < t_{ck}/2$.

12. (currently amended) A method of synchronizing a clock signal for an integrated circuit, comprising:

a) providing an internal clock signal (CIN), an inverted internal clock signal (CIN'), and a clock delay signal (CDLY) having timing characteristics;

b) determining a plurality of phases based upon the timing characteristics of CIN and CDLY;

c) for at least one phase, directing CIN' into a synchronous mirror delay (SMD) such that a reduced number of delay stages are achieved;

wherein the timing characteristics define a period of CIN as t_{ck} and also define from a rising edge in CIN to a rising edge in CDLY as t_{mdl}, and ~~wherein~~ directing occurs when $t_{mdl} < t_{ck}/2$;

d) multiplexing an input with an input selection multiplexor to select whether to direct the CIN or CIN' into the SMD, based on the phase determined in the determining step; and

e) multiplexing, with an output selection multiplexor, an output of the input selection multiplexor with a SMD output, the output selection multiplexor selecting whether to output, based on the phase determined in the determining step, the SMD output or CIN bypassing the SMD, as an input to a clock tree to generate an internal clock signal.

13. (currently amended) A memory device, comprising:

a synchronous mirror delay (SMD); and

a phase detector in electronic communication with the SMD~~, the phase detector~~ and comprising:

means for receiving a clock input signal (CIN) and a clock delay signal (CDLY), the CIN and CDLY each having timing characteristics;~~, the phase detector~~ and

means for outputting a pair of branches each having a logical level, ~~wherein~~ the logical levels of the branches ~~define~~ defining a plurality of conditions ~~of CIN and CDLY~~ based on the timing characteristics of CIN and CDLY; ~~and~~

wherein for at least one of the plurality of conditions, the memory device comprises means for reducing a number of delay stages ~~is reduced~~ for a selected signal to pass through the ~~memory device~~ SMD based on one of the plurality of conditions.

14. (currently amended) The memory device of claim 13 wherein the timing characteristics include a period of CIN defined as t_{ck} and a rising edge from CIN to a rising edge in CDLY is defined as t_{mdl}; and

~~wherein~~ a first phase is when $t_{mdl} > t_{ck}/2$;

~~wherein~~ a second phase is when $t_{mdl} < t_{ck}/2$;

~~wherein~~ a third phase is when $t_{mdl} = t_{ck}$; and

~~wherein~~ a fourth phase is when $t_{mdl} = t_{ck}/2$.

15. (previously presented) The memory device of claim 14 wherein when $t_{mdl} < t_{ck}/2$ the number of delay stages in the SMD is comparable to when $t_{mdl} > t_{ck}/2$.

16. (previously presented) The memory device of claim 14 wherein the number of delay stages when $t_{mdl} < t_{ck}/2$ is reduced by substantially one-half.

17. (previously presented) The memory device of claim 14 wherein the number of delay stages when $t_{mdl} < t_{ck}/2$ is reduced from 128 to substantially 59.

18. (currently amended) A synchronous mirror delay system, comprising:

a synchronous mirror delay (SMD); and

a phase detector ~~associated~~ in electronic communication with the SMD~~, the phase detector~~ and comprising:

means for receiving a clock input signal (CIN) and a clock delay signal (CDLY), the CIN and ~~the~~ CDLY each having timing characteristics; and ~~, the phase detector~~

means for outputting a pair of branches each having a logical level, ~~wherein~~ the logical levels of the branches ~~define~~ defining a plurality of conditions based on the timing characteristics of CIN and CDLY; ~~, and~~

wherein for at least one of the plurality of conditions, the system comprises means for reducing a number of delay stages ~~is reduced~~ for a selected signal to pass through the ~~system~~ SMD based on one of the plurality of conditions, ~~; wherein~~ the timing characteristics define a period of CIN as t_{ck} and also define a period from a rising edge in CIN to a rising edge in CDLY as t_{mdl}, and ~~wherein~~ the plurality of conditions include:

a first phase when $t_{mdl} > t_{ck}/2$;

a second phase when $t_{mdl} < t_{ck}/2$;

a third phase when $t_{mdl} = t_{ck}$; and

a fourth phase when $t_{mdl} = t_{ck}/2$;

means for reducing ~~wherein~~ the number of delay stages in the second phase ~~is reduced~~; and

means for CIN to bypass the SMD ~~wherein~~ in the third and fourth phases~~, CIN bypasses the SMD~~.

19. (currently amended) A synchronizing circuit for use with an integrated circuit, comprising:

an input buffer comprising means for receiving ~~the~~ an external clock signal to produce a clock input signal (CIN), an inverted clock input signal (CIN'), and a clock delay signal (CDLY), each having timing characteristics;

a synchronous mirror delay (SMD) having a measurement delay line input for connection to a measurement delay line, a measurement delay line output connected to a variable delay line input for connection to a variable delay line, the variable delay line including a variable delay line output; and

a phase detector disposed between the input buffer and the SMD, the phase detector having a first input means for receiving the CIN, a second input means for receiving the CDLY, ~~the phase detector~~ means for generating one of a plurality of output signal combinations, each combination corresponding to a phase of the CIN and CDLY signals based on the timing characteristics, means for connecting a CDLY SMD input ~~connected~~ to the measurement delay line input, ~~and~~ means for connecting a SMD output connected to the variable delay line output, and a circuit selectively inputting CIN or CIN' as a CIN SMD input based on the phase of the signals, ~~and~~ wherein for at least one of the phases, a number of delay stages is reduced for the external clock signal ~~a selected signal~~ to pass through the ~~circuit~~ SMD.

20. (currently amended) The circuit of claim 19 wherein the timing characteristics define a period of CIN as t_{ck} and also define a period from a rising edge in CIN to a rising edge

in CDLY as t_{mdl}, and ~~wherein~~ when $t_{mdl} < t_{ck}/2$, CIN' is input into the SMD and when $t_{mdl} > t_{ck}/2$ CIN is input into the SMD.

21. (previously presented) The circuit of claim 20 wherein the number of delay stages in the SMD when $t_{mdl} < t_{ck}/2$ is reduced.

22. (previously presented) The circuit of claim 20 wherein the number of delay stages in the SMD when $t_{mdl} < t_{ck}/2$ is reduced from 128 to substantially 59.

23-25. (canceled)

26. (currently amended) A ~~phase detection and selection~~ system, comprising:

a phase detector comprising means for receiving a clock input signal (CIN) and a clock delay signal (CDLY), each signal having timing conditions, and means for generating a plurality of output signal combinations, each combination based upon the timing conditions; and

logic ~~associated~~ in electronic communication with the phase detector to select one of the output signal combinations corresponding to the timing conditions of the signals;

wherein ~~a phase detection and selection circuit~~ the system selectively feeds CIN or an inverted clock input signal (CIN') into a synchronous mirror delay ("SMD") based upon the plurality of output signal combinations ~~and wherein~~ to reduce a number of delay stages ~~is reduced~~ for a selected signal to pass through the ~~system~~ SMD.

27. (currently amended) The system of claim 26 wherein the timing characteristics include a period of CIN defined as t_{ck} and a rising edge from CIN to a rising edge in CDLY is defined as t_{mdl}; and ~~wherein~~ the phases include:

a first phase when $t_{mdl} > t_{ck}/2$;

a second phase when $t_{mdl} < t_{ck}/2$;

a third phase when $t_{mdl} = t_{ck}$; and

a fourth phase when $t_{mdl} = t_{ck}/2$.

28. (previously presented) The system of claim 27 wherein the number of delay stages is reduced.

29. (previously presented) The system of claim 27 wherein the number of delay stages is reduced substantially by one-half.

30. (previously presented) The system of claim 27 wherein the number of delay stages in the SMD when $t_{mdl} < t_{ck}/2$ is reduced from 128 to substantially 59.

31-33. (canceled)

34. (currently amended) A system, comprising:

a processor;

a memory controller;

a plurality of memory devices;

a first bus interconnecting the processor and ~~the~~ memory controller;

a second bus interconnecting the memory controller and the plurality of memory devices;

each of the memory devices having:

a synchronous mirror delay (SMD);

a phase detector comprising means for receiving a clock input signal (CIN) and a clock delay signal (CDLY), each signal having timing conditions~~, and~~ including a period of CIN (t_{ck}) and a period from a rising edge in CIN to a rising edge in CDLY (t_{mdl}); and means for generating a plurality of output signal combinations, each combination corresponding to phases of the signals based upon the timing conditions; and

logic ~~associated~~ in electronic communication with the phase detector to select one of the output signal combinations corresponding to the timing conditions of the signals to input CIN into the SMD when $t_{mdl} > t_{ck}/2$ and input CIN' into the SMD when $t_{mdl} < t_{ck}/2$ to reduce a number of delay stages in the SMD ~~signals;~~

~~wherein the timing conditions include a period of CIN (t_{ck}) and a period from a rising edge in CIN to a rising edge in CDLY (t_{mdl}) and wherein inputting CIN into the SMD when $t_{mdl} > t_{ck}/2$ and inputting CIN' into the SMD when $t_{mdl} < t_{ck}/2$ reduces a number of delay stages in the SMD~~.

35-81. (canceled)